REMARKS

Claim 1 was rejected as anticipated by Renner. It is respectfully submitted that the following elements set forth in the claim are not found in Renner: (1) an input processor that processes input signals to the digital signal processor; (2) an output processor that processes output signals from the digital signal processor; and (3) a storage selectively accessible by each of the processors.

The office action indicates that the input processor is the element 12 in Figure 1, but it is respectfully submitted that this could not possibly be the case because, as shown in Figure 1, the I/O port is on the lower right hand of the figure and is nowhere close to the item 12. Thus, it is clear that the item 12 does not process input signals. The item 12 is an array controller and sequencer which operates as the master of the array processor and controls the instruction flow therein.

The office action suggests that the output processor is the element 20a but, again, this cannot be so because, again, the I/O port is in the bottom right hand corner of the figure and is nowhere close to the item 20a. Instead, the item 20a is described at column 3, lines 29-31, as a vector address generator. A vector address generator is not a processor which processes output signals from the digital signal processor.

Finally, it is suggested in the office action that the storage selectively accessible by each of the processors is the external ROM, citing column 3, lines 23-26. However, the external ROM is not indicated as being accessible by each of the processors. Each of the processors would be the programmable, multiply and accumulate mathematical processor, the input processor, the output processor, and the master processor. Nothing in the cited material suggests that the ROM is accessible by anything other than the ACS 12. Note that the items 20a, 20b, and 20n have their own separate code section indicated as microcode 30. Thus, if the Examiner still believes that these items are the output processor, there is no reason to believe that they have any way of accessing the so-called external ROM which is the item 40. In addition, the array controller 12 has its own microcode storage 14. There is no reason to believe that the microcode 14 is accessible by anything other than the array controller.

Therefore, reconsideration is respectfully requested.

Claim 2 calls for a random access memory processor that stores intermediate calculation results. It is suggested in paragraph 4 of the office action that this is the element 20b. However, nothing indicates that the code store 30 is randomly accessible. Since what is stored there is microcode 30, there is no particular reason to believe that it is randomly accessible. At line 37 of column 3, the microcode 30 is called "ROM resident." This would further suggest that it is not randomly accessible.

Claim 3 calls for a bus coupling each of said processors to the storage. The office action does not point out where such buses might possibly be. Therefore, reconsideration is respectfully requested.

Concerning claim 4, since there are no input and output processors, there are no such processors that implement mathematical operations.

With respect to claim 5, it is suggested in the office action that the Abstract indicates that each of the asserted processors have their own instruction sets. However, all that the Abstract indicates is that data instructions are sequenced through in accordance with sequenced commands by the master controller 12. This does not suggest that each of the so-called processors have instructions, much less their own instruction sets. Therefore, reconsideration is requested.

Claim 6 calls for each of the processors to communicate with one another through said storage. The material at column 3, lines 23-26, does not describe such a communication system.

Claim 8 calls for each of the processors to receive timing from the master processor. The material cited in support thereof, column 3, lines 13-25, does not discuss any kind of timing. Therefore, reconsideration is requested.

Claim 9 calls for the master processor to wait for the input processor to complete a given operation. It is suggested that it is inherent because the system is clocked. Just because a system is clocked does not mean that it needs to be sequential in the fashion claimed. Therefore, reconsideration is requested.

Claim 10 calls for each of the processors to have its own random access memory. It is suggested that Renner teaches this, citing element 132 of Figure 4 and element 202 of Figure 5, element 220 and inherent in element 10.

The element 132 is described at column 6, lines 54-56. Nothing indicates that it is randomly accessible.

The item 202 is described as a parameter register file at lines 34 and 35 of column 8. However, nothing indicates that it is randomly accessible. Similarly, nothing indicates that the element 220 is randomly accessible. The item 220 is a multiplier file and it is not even seen why it would be believed that it would be randomly accessible.

It is suggested that the item 10 is inherently randomly accessible. However, it is not seen why this is so. The only discussion of any stored code is ROM stored code which would not be randomly accessible. Therefore, reconsideration of the rejection of claim 10 is respectfully requested.

In the present application, a multi-cycle arithmetic element uses a busy signal to hold off new data from being sourced to the arithmetic element 98. See page 24 of the specification at lines 15-19. Thus, it does not appear that anything in the cited reference constitutes a multi-cycled mathematical processor set forth in claim 15. Therefore, reconsideration is requested.

Claim 7 was rejected as obvious over Renner taken alone. It is not understood how a single reference could establish a *prima facie* obviousness rejection. Necessarily, the reference is missing something and it cannot teach that very missing thing. While arguments are made about how good it would be to have very long instruction words in Renner, there is no reason to believe that Renner could have accommodated very large instruction words or that he ever thought to use them. Therefore, a *prima facie* rejection cannot be made out because nothing in Renner suggests the use of very long instruction words.

Corresponding arguments apply to claims 16-24. Therefore, reconsideration is respectfully requested.

Respectfully submitted,

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